impedance of said non-clocked, non-inverting amplifier chip is approximately 4 to 1.

REMARKS

Claims 11-14 are in the case.

The proposed drawing changes filed on September 11, 2002 have been disapproved. The specification has been objected to as not being sufficiently concise. Claim 10 stands rejected under 35 U.S.C. 112, first paragraph as containing subject matter not described in the specification. Claims 4-10 stand rejected under 35 U.S.C. 112, second paragraph, as being indefinite. Claim 4 stands rejected under 35 U.S.C. 102(b) as being anticipated by Buch. Claims 5 and 7 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Buch. Claims 6 and 8-10 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Buch and Chiang et al. These objections and rejections are respectfully traversed and reconsideration is requested in light of the amendments above and the arguments below.

Appendix A contains a clean copy of the changes to the specification in the preliminary amendment filed on September 11, 2002.

Figures 1A and 1B have been changed by identifying the CPU block, the DSP block, and the CPLD block with reference numbers.

The specification has been redacted and amended to overcome the objection with regard to conciseness. Former figures 4A-5C have been removed, and the succeeding figures have been renumbered accordingly. There is no new matter in these revised drawings.

Claims 4-10 have been cancelled. However, new claim 14 refers to a four to one ratio. Support for this ratio is found in the second full paragraph on page 9 and the following paragraph.

If, at any time, the Examiner in charge of this application feels that prosecution of this application could be expedited through a telephone interview, the Examiner is invited to contact the undersigned by telephone at (412) 380-0725.

Respectfully Submitted,

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APPENDIX A

Title of the Invention:

PROGRAMMABLE SYSTEM INCLUDING SELF LOCKING MEMORY CIRCUIT FOR A TRISTATE DATA BUS

In the Specification:

Insert a heading immediately after the Title of the Invention, and before the first full paragraph on Page 1 of the Substitute Specification reading as follows:

CROSS REFERENCE TO RELATED APPLICATIONS

***

First full paragraph after the Title of the Invention on Page 1 of the Substitute Specification:

This application claims priority under 35 U.S.C. §119(e) from Provisional Application Serial No. 60/109,951, filed on November 25, 1998 and entitled "Intelligent Door Controller Unit". This Provisional Application is assigned to Westinghouse Air Brake Company, the assignee of the present application, and is incorporated herein by reference thereto.

***

Paragraph spanning Pages 1 and 2 of the Substitute Specification:

In the above-noted provisional application, a self-locking circuit is shown connected to a tri state bit line of a data bus interconnecting a central processing unit (or "CPU") and other digital transceiving processing devices, such as a Motion Control Digital Signal Processor (or "DSP"), to provide a memory of the last data value or electrical potential sent on such line, i.e., the last read or write transfer between the CPU and the processing devices. The line is said to be "tri state" because of the three voltage states which the line can assume, namely, a high voltage state, a low voltage state and a state in which no current flow is generated.

***

Second full paragraph on Page 2 of the Substitute Specification:

The present invention uses a known, commercially available, non-inverting, non-clocking buffer amplifier chip and a simple parallel resistor connected across the chip, i.e., connected to the input and output terminals of gates of the chip. These two means (chip and resistor) when connected to a tri state bit line provide a predetermined relatively high impedance on the line that is effective in latching the latest value found on the line.

***

Please replace the first full paragraph in the section entitled "BRIEF DESCRIPTION OF THE DRAWINGS" of the substitute specification to read as follows:

Figures 1A and 1B, taken together, present a schematic diagram showing eight buffer memory latching circuits of a presently preferred embodiment of the invention and their connection to the bit lines of an eight bit data bus.

***

First full paragraph on Page 6 of the Substitute Specification:

Reference is now made, more particularly, to the drawings. Figures 1A and 1B together show eight buffer memory circuits, generally designated 220, electrically connected, respectively, to eight tri state bit lines 0 through 7 of a data bus 9 interconnected between tranceiving digital components 20 and 30. An example of such an interconnection of components is the central processing unit (or "CPU") 230, the Motion Control Digital Signal [Motion Control] Processor (or "DSP") 320 and the Complex Programmable Logic Device (or "CPLD") 300 interconnected in the read/write manner shown in Figures 7B and 10B of the above incorporated provisional patent application.

***

Paragraph spanning Pages 6 and 7 of the Substitute Specification:

More particularly, circuit 220 of the invention comprises a digital buffer amplifier chip 10 and a parallel resistor 12 connected across the chip 10 such that the input and output terminals 14 and 16 of the chip 10 (only schematically shown in the figures) are connected together by the resistor. Chip 10 is a well known, commercially available, non-inverting digital amplifier having no clocking elements. Its input terminal 14 is connected to a bit line, namely, bit line 4 in Figure 2. As such, in the circuit 220, the signal or potential newly applied to input 14 of the chip 10 from the bit line is retained after current in the line builds to a predetermined threshold level for circuit 220.

PROGRAMMABLE SYSTEM INCLUDING SELF LOCKING MEMORY CIRCUIT FOR A TRISTATE DATA BUS

CROSS REFERENCE TO RELATED APPLICATIONS

This application claims priority under 35 U.S.C. §119(e) from Provisional Application Serial No. 60/109,951, filed on November 25, 1998 and entitled "Intelligent Door Controller Unit". This Provisional Application is assigned to Westinghouse Air Brake Company, the assignee of the present application, and is incorporated herein by reference thereto.

FIELD OF THE INVENTION

The present invention relates, in general, to memory circuits and, more particularly, this invention relates to the details of a simple, self-locking memory circuit for a ~~tri state~~tristate bit line of a data bus.

BACKGROUND OF THE INVENTION

In the above-noted provisional application, a self-locking circuit is shown connected to a ~~tri state~~tristate bit line of a data bus interconnecting a central processing unit (or "CPU") and other digital transceiving processing devices, such as a Motion Control Digital Signal Processor (or "DSP"), to provide a memory of

the last data value or electrical potential sent on such line, i.e., the last read or write transfer between the CPU and the processing devices. The line is said to be "~~tri state~~tristate" because of the three voltage states which the line can assume, namely, a high voltage state, a low voltage state and a state in which no current flow is generated.

The self-locking circuit of the invention is useful on any connecting bit line where it is desirable to latch and hold the last value or state on the line and thereby retain and maintain such value once the driver relinquishes control of the line, i.e., when the line returns to a high impedance state.

SUMMARY OF INVENTION

The present invention uses a known, commercially available, non-inverting, non-clocking buffer amplifier chip and a simple parallel resistor connected across the chip, i.e., connected to the input and output terminals of gates of the chip. These two means (chip and resistor) when connected to a ~~tri state~~tristate bit line provide a predetermined relatively high impedance on the line that is effective in latching the latest value found on the line.

More particularly, a circuit device supplying the bit line with a signal has a relatively low impedance. The relatively low impendence of the supply device and the relatively high impedance of the latching circuit of the invention provides a voltage divider

that produces a low voltage at the supply circuit while the high impedance of the latching circuit develops a relatively high voltage.

When the signal from the supply device or circuit goes from a low state to a high state, the output voltage of the latching circuit is at a low state. Thus, the input voltage to the amplifier chip and resistor of the latching circuit of the invention initially rises to the voltage divided level. At a certain voltage threshold, the latching circuit switches to the high state, with the output terminal of the chip now also being in a high state. The latching circuit now has essentially the same high state as the output of the supplying (or sending) circuit.

Since the chip has no clocking elements, it is stable over time and holds the value received from the sending circuit. It will not switch until such time as a new value is imposed on the input terminal of the latching circuit at a level that moves through a low voltage threshold value to return the circuit to a low state. Again, the circuit will hold this "low" value until it is forced to change by a new "high" state sent on the bit line and imposed upon the latching circuit.

In the above incorporated provisional patent application, for example, the timing structures of the CPU and DSP are different. By holding data over time, the circuit of the present invention

allows the CPU and DSP to work together while simultaneously preventing noise on the bit line from being transferred between the CPU and DSP, i.e., the impedance of the circuit of the invention temporarily changes (lowers) only when the latest value or state on the bit line builds or lowers to a current level above or below the threshold levels of the circuit, after which the chip of the circuit conducts. When this occurs, the impedance of the circuit temporarily falls to a low value, temporarily loads the line, then returns to the relative high impedance value to hold the new, latest value and to remove the load from the line. In this manner, the circuit is self-locking and resists transferring noise and electromagnetic interference, as such noise and interference do not sustain current levels sufficient to force the switching of the circuit.

OBJECTS OF THE INVENTION

It is, therefore, one of the primary objects of the present invention to provide a simple digital latching circuit for retaining the latest information (high or low state) conveyed on a bit line.

Another object of the present invention is to provide a data latching circuit that requires no clocking, timing or synchronization pulses to latch the data.

Yet another object of the present invention is to provide a means for testing the integrity of a printed circuit board bus signal.

Still another object of the present invention is to use a commercially available, non-inverting digital amplifier chip and an electrical resistor connected across the chip as the latching circuit of the invention, with the chip and resistor providing a predetermined impedance for such latching circuit.

A further object of the present invention is to provide a digital circuit having the capability of extending the hold times of data conveyed on bit lines connected between digital circuit devices.

Yet another object of the present invention is to provide a circuit that exhibits a substantial reduction in noise and interference for ~~tri state~~tristate digital bit lines.

In addition to the specific objects and advantages of the present invention described above, various other objects and advantages of the invention will become more readily apparent to those persons who are skilled in the relevant memory circuit art from the following more detailed description of the invention, particularly when such description is taken in conjunction with the attached drawing Figures and with the appended claims.

BRIEF DESCRIPTION OF THE DRAWINGS

Figures 1A and 1B, taken together, present a schematic diagram showing eight buffer memory latching circuits of a presently preferred embodiment of the invention and their connection to the bit lines of an eight bit data bus~~.~~;

Figure 2 is a circuit diagram useful in explaining the operation of the presently preferred embodiment of the latching circuit of the present invention~~.~~;

Figure 3A illustrates a typical passenger transit train including the central door controller (CDC) in the lead railcar, the door controller units (DCUs) on each railcar to which the CDC is linked, and the door operator(s) which each DCU drives~~.~~;

Figure 3B is a perspective view of one type of door operator installed over a doorway whose doors are shown open~~.~~;

Figure 3C is a perspective view of the door operator of Figure 2 with the doors shown closed over the doorway~~.~~

~~Figures 4A-C are frontal views of the left door lock assembly of Figures 2-3 showing its lock member in the unlocked, pushback-locked and fully-locked states, respectively.~~

~~Figures 5A-C are frontal views of the right door lock assembly of Figures 2-3 showing its lock member in the unlocked, pushback-locked and fully-locked states, respectively.~~

~~Figure 6;~~

Figure 4 is a simple block diagram of an intelligent door controller unit (IDCU) according to the invention.

Figures ~~7A-B~~5A-B illustrate an expanded version of the block diagram of Figure ~~6~~4 showing a preferred modular architecture for the IDCU inclusive of a CPU card, a power supply card, and a motor driver & input/output (MD-I/O) card~~.~~;

Figure ~~8~~6 illustrates a basic configuration for the IDCU in which a single IDCU is used to control each doorway~~.~~;

Figure ~~9~~7 illustrates an advanced configuration for the IDCU in which a single CPU card can support multiple MD-I/O cards to control multiple doorways~~.~~;

Figures ~~10A-C~~8A-C illustrate a circuit layout for the MD-I/O card shown in Figures ~~7A-B~~5A-B inclusive of a mirror-image optoisolator device, complex programmable logic devices (CPLDs), a motion control processor and an H-bridge amplifier~~.~~;

Figure ~~11~~9 is a schematic of a mirror-image optoisolator circuit and the two mirror-image registers to which it writes in the input/output (I/O) CPLD on the MD-I/O card~~.~~;

Figures 1~~2~~0A-C illustrate one possible scheme for the I/O-CPLD and related circuits on the MD-I/O card~~.~~;

Figure 1~~3~~1 illustrates one possible scheme for the address (ADD) CPLD and related circuits on the MD-I/O card~~.~~; and

Figures 1~~4~~2A-E illustrate one possible scheme for the motor control (MC) CPLD and related circuits on the MD-I/O card.

BRIEF DESCRIPTION OF A
PRESENTLY PREFERRED EMBODIMENT

Reference is now made, more particularly, to the drawings. Figures 1A and 1B together show eight buffer memory circuits, generally designated 220, electrically connected, respectively, to eight tristate bit lines 0 through 7 of a data bus 9 interconnected between transceiving digital components 20 and 30. An example of such an interconnection of components is the central processing unit (or "CPU") 230, the Motion Control Digital Signal Processor (or "DSP") 320 and the Complex Programmable Logic Device (or "CPLD") 300 interconnected in the read/write manner shown in Figures 5B and 8B of the above incorporated provisional patent application.

The buffer memory circuit of the invention bears the same reference numeral (220) found in the above application. The buffer memory of the present invention, however, has utility on any data bus or digital circuit where memory of the last transfer of data requires retention and can be used on any number of bit lines.

The eight circuits 220 which are illustrated in Figures 1A and 1B are substantially identical so that only one of the circuits is discussed herein in detail. This circuit is shown, in Figure 2 of

the drawings, connected to a bit line 4 extending between the two digital circuits 20 and 30.

More particularly, circuit 220 of the invention comprises a digital buffer amplifier chip 10 and a parallel resistor 12 connected across the chip 10 such that the input and output terminals 14 and 16 of the chip 10 (only schematically shown in the figures) are connected together by the resistor. Chip 10 is a well known, commercially available, non-inverting digital amplifier having no clocking elements. Its input terminal 14 is connected to a bit line, namely, bit line 4 in Figure 2. As such, in the circuit 220, the signal or potential newly applied to input 14 of the chip 10 from the bit line is retained after current in the line builds to a predetermined threshold level for circuit 220.

~~The buffer memory circuit of the invention bears the same reference numeral (220) found in the above application. The buffer memory of the present invention, however, has utility on any data bus or digital circuit where memory of the last transfer of data requires retention and can be used on any number of bit lines.~~

~~The eight circuits 220 which are illustrated in Figure 1 are substantially identical so that only one of the circuits is discussed herein in detail. This circuit is shown, in Figure 2 of the drawings, connected to a bit line 4 extending between the two digital circuits 20 and 30.~~

~~More particularly, circuit 220 of the invention comprises a digital buffer amplifier chip 10 and a parallel resistor 12 connected across the chip 10 such that the input and output terminals 14 and 16 of the chip 10 (only schematically shown in the figures) are connected together by the resistor. Chip 10 is a well known, commercially available, non-inverting digital amplifier having no clocking elements. Its input terminal 14 is connected to a bit line, namely, bit line 4 in Figure 2. As such, in the circuit 220, the signal or potential newly applied to input 14 of the chip 10 from the bit line is retained after current in the line builds to a predetermined threshold level.~~

The circuit operates in the following manner:

The input to circuit 220, in Figure 2, is received from a digital circuit device represented schematically by an amplifier symbol 20 and a resistor 22. Resistor 22 represents the internal output impedance of amplifier 20 and is determinative of its output voltage. The electrical output impedance of amplifier 20 is relatively low in comparison to that of resistor 12 of latching circuit 220 such that any voltage developed by amplifier 20 divides at the connection 24 of the two resistors 22 and 12, with the greater of the two voltages being developed across resistor 12.

For example, if amplifier 20 produces a five volt signal, it can divide on a one and four volt basis, with the four volts being

applied to the input terminal 14 of chip 10. The present state of chip 10, however, may be at zero volts, i.e., zero volts at its input and output terminals 14 and 16. Output terminal 16 and a series resistor 26, which represents the internal impedance of chip 10, are a virtual ground or virtual Vcc for circuit 220. Resistances 12 and 26 represent the total impedance of circuit 220 of the invention.

In the case of amplifier 30, as schematically presented, a resistor 32 is shown in Figure 2 that represents the internal impedance of the amplifier 30.

Circuit 220 has a voltage threshold level that permits the circuit to change states. If the divided voltage is at the threshold level, circuit 220 switches to a state where its input and output terminals 14 and 16 are now at a "high" state, such as the above divided four volt level. This occurs by chip 10 momentarily conducting, thereby momentarily loading the bit line, bit line 4, for example. As soon as the chip 10 conducts and goes "high", conduction and loading of the bit line 4 ceases. Being a non-inverting device, chip 10 does not change the state or potential of the latest signal applied thereto.

In the drawing figures, amplifier symbol 20 is shown as a ~~tri state~~tristate bus driver but it is also a ~~tri state~~tristate receiver, as indicated by a second amplifier symbol 20A. The third

amplifier (symbol 30) is also a bus receiver and driver, the dual function being again indicated by a second amplifier symbol 30A. In the read/write arrangement of the CPU and DSP in the above noted provisional application, the driver/receiver functions are interchangeable such that amplifier 30 can be the driver and amplifier 20 the receiver. In either case, circuit 220 holds the latest potential supplied on the bit line until one of the two, upper and/or lower thresholds of circuit 220 are crossed.

In crossing the lower threshold of circuit 220, amplifier 20 or 30 will place a "low" potential on the bit line while the other circuit is in a high state. Circuit 220, which is presently latched in a high state, tries to maintain the high state. However, when the voltage on input terminal 14 of chip 10 drops through the low threshold before the chip 10 conducts and switches to the low state, the chip 10 temporarily and momentarily loads the bit line 4. As the output 16 of the chip 10 changes state, the chip 10 immediately thereafter ceases conducting, unloads the bit line 4 and holds the new "low" state until such time that its upper threshold is reached, which occurs when a "high" voltage is received at input terminal 14.

Circuit 220 loads the bit line only when it switches (i.e. when chip 10 conducts) which makes the circuit 220 highly effective in resisting electromagnetic noise and interference, as such noise

and interference can not sustain current flow and a voltage level sufficient to reach the switching thresholds of the circuit 220.

Further, the circuit 220 does not oscillate, as there is no phase shift between the input 14 and output 16 of chip 10. The circuit 220 is a digital device having only high and low states. The circuit 220 latches and locks itself until its thresholds, high and low, are reached by a new state on the bit line.

In this manner, circuit 220 retains the latest information until it is forced to change, as per above. If the circuit 220 does not retain the last bit of information (potential), it is an indication of current leakage on the circuit board (not shown) on which chip 10 and resistor 12 are mounted. Circuit 220 thereby provides, in addition, an internal diagnostic function on the board. It alerts a technician of such a problem so that he or she can proceed to find the location of the leakage.

Because the circuit 220 extends hold times of data, it functions to match the timing of respective devices interconnected by bit lines that transfer data, such as the amplifiers 20 and 30, or the CPU and DSP devices described in the above incorporated patent application and described below. As noted above, the CPU and DSP do not have a one hundred percent match in their timing requirements.

The following background information is provided to assist the reader to understand the environment in which the invention will be used. The terms used herein are therefore not intended to be limited to any particular narrow interpretation unless specifically stated otherwise in this document.

Shown in Figure 3A is a typical passenger transit train. It has a lead railcar 41 and a plurality of trailing railcars 41 each linked serially by means of a mechanical coupler. Various electrical trainlines span the length of the train. Each trainline is composed of a series of interconnected wires, with each such wire contained (along with the wires of the other trainlines) within a protective conduit secured to the underside of each railcar. Each such conduit connects via an electrical connector to another such conduit on a neighboring railcar so as to extend each trainline along the train. These trainlines are used to carry the electrical signals that are needed to operate and control the various systems on each of the railcars in the train.

~~Each railcar has its own power distribution network (LVDN) from which it provides the relatively low voltage needed to power all of the electrical/electronic systems on the vehicle. The power level provided the LVDN typically ranges from 12 to 150V dc (52V dc nominal), depending on the particular type of railcar at issue and the power requirements imposed by the passenger transit authority.~~

Like the lead railcar, each of the trailing railcars may be equipped with one or more motors and a propulsion controller unit with which to control them. ~~These propulsion controllers are connected by one or more trainlines to a master controller unit (MCU) located in the lead railcar. From the controls of the master controller, a train operator can control, in addition to the mechanical brakes on each railcar, the operation of all of the propulsion controllers in the train. It is thus from the master controller that the train operator can operate the motors on each railcar in unison to propel or electrically brake the train. The propulsion system of the train is also linked to another trainline known as the traction confirmation (TC) trainline 36. As is known in the passenger transit industry, the propulsion system deprives its motors of the ability to propel the train whenever the TC trainline 36 is open circuited.~~

Each transit railcar has one or more openings or doorways 37 through which passengers can enter and exit the railcar. ~~For railcars with more than one doorway, the openings may be located in the same sidewall or opposite sidewalls of the vehicle.~~ Over each doorway 37 is installed a door hardware system (DHS), also referred to as a door operator 40, to which the door panel(s) attach. The door operator is what actually moves the door panel(s) back and forth over the doorway to open and close the doors, depending on

whether its motor is commanded to rotate in the opening or closing direction. ~~The type of door operator selected to be installed on a railcar, of course, affects the dimensions of and accoutrements required for the opening. Plug doors, pocket doors, outside sliding doors and station platform doors are just some examples of the types of door systems currently being used in the transit industry.~~

In addition to the propulsion motors, the doors of the railcars in a passenger train are also centrally controlled from the lead railcar. Specifically, a central door controller (CDC) 33 housed in the lead railcar communicates with, and controls, one or more door controller units (DCU) 74 on each railcar through a number of discrete door control trainlines. Each DCU 74 controls one or more door operators 40, and their associated motors~~, based on the input signals that it receives from two sources: (1) the central command signals received from the CDC 33 and (2) the local door hardware signals received from the door operator(s) 40 and related hardware.~~

~~Along the door control trainlines, many passenger transit authorities convey most, if not all, of the following central command signals from the CDC: door unlock, door open, door close, door lock, side select enable, cliff side select enable, zero speed, and low speed. The zero speed, low speed and cliff side~~

~~select enable signals may alternatively be generated by each railcar and thus provided to each DCU locally. The zero speed signal, when present, indicates that the train has come to a complete stop. The low speed signal indicates that the speed of the train (i) upon acceleration is now high enough to allow the doors to be locked or (ii) upon deceleration is now low enough to allow the doors to be unlocked. Another trainline --the park brake trainline-- can be used to convey an enabling/disabling signal to the DCU either from the railcar locally or from the CDC via routers. This trainline is used to inform the DCU whether the parking brake(s) of the railcar/train has been engaged. Yet another trainline --the passenger control trainline-- can be used to convey an enabling/disabling signal to the DCU either from the CDC or from the railcar locally. It is used to enable or disable the passenger request open/hold push button switches, described below, by which passengers can request the DCU 74 to open or hold open the doors.~~

~~As there are many different door systems in use today, not every transit authority uses every one of the aforementioned central command signals. For example, in some systems, the door unlock and lock signals may be subsumed by the door open and close signals, respectively. Another example would be a train composed of railcars whose doorways are located in the same sidewall. In this~~

~~instance, the side select trainline would be unnecessary, as it is normally used only on trains whose railcars have doorways 37 on both sides. In dual-sided railcars, this trainline allows doors to be selectively disabled on one or the other side of the train.~~.

Specifically, each door operator 40 is deployed with one or more door lock solenoids and a side select emergency lockout solenoid, both controllable by the DCU 74 in response to the side select signal. ~~When so commanded by the CDC 33, the DCUs will activate the door lock and lockout solenoids on the selected side so as to lock the doors and physically disable the INT EMER door release handles (see below) on that side of the train. The side select trainline is typically used in transit systems whose train station platforms are not always on the same side of the train.~~

The local door hardware signals that the DCU 74 receives typically come from switches that are used to sense the status of the doors. Such door status switches are typically part of the door operator assembly 40, though they may also be added to the door hardware subsequently. Most of these switches have two contacts, the first contact of each switch being used to provide an input to the DCU. Each switch is dedicated to sensing whether or not a particular part of the door operator/DHS 40 has assumed a given state. ~~Examples of such switches used in prior art systems include: (i) the door close limit switch(es) whose contacts when~~

~~closed indicate that the door panels have been closed to at least a partially closed position; (ii) the door lock switch(es) whose contacts when closed indicate that the doors are locked; (iii) the EXT EMER door release switch which when opened indicates that the external emergency door release handle has been used to open the doors; and (iv) the INT EMER door release switch which when opened indicates that the internal emergency door release handle has been used to open the doors.~~

~~The~~

A cliff side select trainline is used by many transit authorities to selectively disable (i.e., physically lockout) the INT EMER door release handles on one or both sides of the train. ~~This feature is employed mostly on subway or elevated passenger trains, as an added safety feature. On each side of a railcar, each of the INT EMER door release handles are deployed with a bi-stable lockout assembly that is controlled by the DCU 74 in response to the cliff side select signal.~~ Each lockout assembly includes a bi-stable relay, a movable plunger and a locking pin connected to the plunger. ~~When so commanded by the CDC 33, the DCUs will command each of the bi-stable relays to assume an unlock state, a stable state in which the relays will remain even if power is lost. This causes their plungers, and the locking pins therewith, to move to an unlock position in which the INT EMER door~~

~~release handles on the selected side(s) of the train can be used to open the doors. Conversely, when so commanded by the CDC, the DCUs will command each of the bi-stable relays to assume a lock state, also a stable state. This causes their plungers, and their locking pins, to move to a lock position thereby physically disabling the INT EMER door release handles. Should a subway train or elevated train suffer a loss of power away from a station, the cliff side select trainline can thus be used to prevent the passengers, for their safety, from using the INT EMER door release handles to open the doors. Their rescuers, of course, would still be able to open the doors using the EXT EMER door release handles.~~

~~On each railcar, those door status switches having two contacts have their second contact wired into a separate trainline known as the door close and lock confirmation (DCLC) trainline 38. Each railcar 41 has its own DCLC trainline 38 and at least two routers (R), with one router R connected to each end of the DCLC trainline. The TC trainline 36 of the train is strung in series between these two routers R on each railcar. In a manner well known in the art, whenever any one of the door status switches is open on any railcar, the DCLC trainline 38 on that railcar is not only open circuited but also interacts with its corresponding routers R to open circuit the TC trainline 36. Whenever this occurs, the propulsion system, as noted above, deprives its motors of the~~

~~ability to propel the train. Moreover, whenever any one of the door status switches is open, the DCU 74 is typically used to illuminate a warning lamp on the outside of the affected railcar. This provides a visual indication to the train operator in the lead railcar that the doors on the affected railcar either have a defected switch in its door operator 40 or have not yet closed. Most railcars also have an EMER door cutout switch. Specifically, the EMER door cutout switch has two contacts: the first normally open, the second normally closed. The normally open contact is wired into the DCLC trainline 38 in parallel to most, if not all, of the door status switches. The normally closed contact, however, is wired into the power supply line that provides power from the power distribution network on the railcar to the DCU 74. Should any one of the door status switches fail open and thus prevent the train from moving, the train operator can block the affected doorway by pulling down a lockout bar. When this lockout bar is in place, the contacts of the EMER door cutout switch change state (i.e., the normally open and closed contacts close and open, respectively). With the lockout bar in place, the EMER door cutout switch simultaneously closes the DCLC trainline 38 and disconnects the DCU 74 from its source of power. This permits the train to move, but prevents the DCU 74 from operating the doors over the affected doorway(s) 37.~~

~~Another local door hardware signal that could be used as an input to the DCU(s) comes from the passenger request open/hold push button switch. Unlike the other door status switches, this switch need not have a second contact wired into the DCLC trainline 38. The contact of this switch when closed indicates that a passenger has requested that the doors be opened or held open from either the inside or outside of the railcar. The effect that this switch has on the DCU 74 can be enabled or disabled by the passenger control trainline. Some transit authorities also provide push button switches that the passengers can use to request that the doors be closed.~~

Among the many door operators to which the invention(s) disclosed herein is directed is the door hardware system 35 disclosed in the text and figures of U.S. Patent Application Serial No. 09/099,260, now US Patent 6,032,416. For the sake of clarity, the reference numerals used to denote the door operator hardware herein are the same as those used in the cited document. Figure 3B shows an opening 37 in a sidewall 39 of a railcar 41. Fixed to or incorporated as part of the body of railcar 41 above opening 37 is a base plate 34 disposed just above and horizontally along the length of opening 37. It is to this base plate 34 that the door hardware system 35 attaches to railcar 41.

~~As shown in Figures 3B-5C, the door hardware system 35 features a plurality of rod hangers 90, a motor 76, a drive mechanism 170, a door hanger rod 88, first and second door panels 42 and 110, outer and inner door hangers 46 and 83 for first door 42, inner and outer door hangers 111 and 121 for second door 110, and first and second door lock assemblies 44 and 117 for door panels 42 and 110, respectively. Each of the door panels 42 and 110 has on its inner edge 53 and 114, respectively, a rubber-like strip 52 and 120, respectively, that collectively serve not only as a weather seal but also as a biasing means in the manner described below.~~

The first and second door lock assemblies 44 and 117, as well as motor 76, are attached to the base plate 34 of railcar 41 by means of bolts and brackets. Specifically, motor 76 is bolted to the base plate via an L-shaped bracket. The first door lock assembly 44 is bracketed to base plate 34 above the left vertical edge of opening 37. Similarly, the second door lock assembly 117 is bracketed to base plate 34 above the right vertical edge of opening 37.

Viewed from left to right in Figures 3B and 3C, the drive mechanism 170 includes coupling 77, drive shaft 78, coupling 81, first helical screw 80, center coupling 104, second helical screw 102, and first and second drive nut assemblies 150 and 190, respectively. Controlled by a DCU based on various central command

signals and local door hardware signals, the motor 76, and the gear reducer unit 79 at its right to which it is connected, is what drives the drive mechanism 170. ~~Specifically, coupling 77 couples the output shaft of gear reducer unit 79 to the left end of drive shaft 78. The right end of shaft 78 is coupled to the left end of first screw 80 by coupling 81. Center coupling 104, in turn, couples the right end of first screw 80 to the left end of second screw 102.~~

~~Six rod hangers 90, attached by bolts to the base plate 34 of railcar 41, are used to interconnect the door hanger rod 88 to the railcar base plate. Located just right of coupling 77 is the first rod hanger 90. It features a receptacle in its lower end in which the left end of door hanger rod 88 is secured. Similarly, the sixth rod hanger 90 has a receptacle in its lower end in which the right end of door hanger rod 88 is secured. Each of the first through fifth rod hangers 90 has two orifices, one in its upper end, the other in its lower end. By their lower orifices, these five rod hangers are used to support door hanger rod 88 and the weight that door hanger rod 88 bears. Drive shaft 78 passes through and thus can be rotated within the upper orifice of the first rod hanger 90. Located just right of coupling 81 is second rod hanger 90. First screw 80 passes through its upper orifice and is free to rotate therein. Center coupling 104 is supported by the~~

third and fourth rod hangers 90. Located just left of center coupling 104 is third rod hanger 90. First screw 80 is free to rotate within its upper orifice. The fourth rod hanger 90 is located to the right of center coupling 104. Second screw 102 passes through its upper orifice and is free to rotate therein. Located just left of the second door lock assembly 117 is the fifth rod hanger 90. The right end of second screw 102 is free to rotate within its upper orifice, and does not extend further to the sixth rod hanger 90.

Each door hanger features a lower section that takes the form of a bracket and an upper section that defines a horizontally disposed bore. By their lower brackets, outer and inner door hangers 46 and 83 are affixed by bolts to the top corners of first door panel 42. Similarly, inner and outer door hangers 111 and 121 are affixed by bolts to the top corners of second door panel 110. By their respective bores, the door hangers are each collared around door hanger rod 88. In particular, outer door hanger 46 is collared around rod 88 between the first and second rod hangers 90. Inner door hanger 83 is collared around rod 88 between the second and third rod hangers 90. Inner door hanger 111 is collared around rod 88 between the fourth and fifth rod hangers 90. Outer door hanger 121 is collared around door hanger rod 88 between the fifth and sixth rod hangers 90. Suspended from rod 88 by hangers 90, door

panels 42 and 110 can be slid over the opening 37 in sidewall 39 of railcar 41 between an UNLOCK POSITION at one extreme to an OPEN POSITION at the other extreme, as explained below.

The first drive nut assembly 150 of drive mechanism 170 is bolted to the top of inner door hanger 83 of first door 42. Similarly, second drive nut assembly 190 is bolted to the top of inner door hanger 111 of second door 110. First and second screws 80 and 102 are threaded in opposite directions, with one bearing right-handed threads and the other left-handed threads, yet are configured to rotate in the same direction due to their linkage within drive mechanism 170. The first nut assembly 150 features a threaded drive nut designed to ride along the matching threads of first screw 80 as first screw 80 is rotated. Similarly, the second nut assembly 190 has a threaded drive nut matched to ride along second screw 102 as second screw 102 is rotated. Because screws 80 and 102 bear oppositely directed threads, the first and second drive nuts travel in opposite directions along screws 80 and 102, respectively, no matter which way motor 76 is commanded to rotate. As inner door hanger 83 interconnects the first drive nut and door panel 42, the door 42 by its hangers 46 and 83 will always slide along door hanger rod 88 in the same direction that the first drive nut is driven along the threads of first screw 80. Likewise, as inner door hanger 111 interconnects the second drive nut and door

panel 110, the door 110 by its hangers 111 and 121 will always slide along door hanger rod 88 in the same direction that the second drive nut is driven along the threads of second screw 102. The doors of door hardware system 35 are thus designed as bi-parting doors, with door panels 42 and 110 closing together when motor 76 is commanded to rotate in a closing direction and opening away from each other when motor 76 is commanded to rotate in an opening direction.

Regarding the locking feature of door hardware system 35, each outer door hanger has a contact bracket attached to the top of its upper section. Specifically, attached to the upper section of outer door hanger 46 is contact bracket 47, as shown in detail in Figures 4A-C. Outer door hanger 121 has attached to the top of its upper section contact bracket 123, as shown in detail in Figures 5A-C. These two contact brackets are mirror-symmetrical parts, so only one bracket need be described. Contact bracket 47 features a contact block 48 and a protuberance 65. Atop outer door hanger 46, contact bracket 47 is designed to cooperate with first door lock assembly 44 to provide a lock for door panel 42. Similarly, second door lock assembly 117 cooperates with contact bracket 123, atop outer door hanger 121, to provide a lock for door panel 110.

First and second door lock assemblies 44 and 117 are also mirror-symmetrical devices. For this reason, the parts of second door

~~lock assembly 117 are not described in detail for the sake of brevity. Reference can also be had to the figures of U.S. Patent Application Serial No. 09/099,260, now US Patent 6,032,416. As shown in Figures 4A-C, first door lock assembly 44 includes lock member 43, pivot pin 45, unlock actuator (denoted by 49 or 50), pushback member 59, latch lever 62, emergency release rotor 64, full lock switch 56 and pushback lock switch 58. As shown in Figures 5A-C, second door lock assembly 117 includes lock member 122 and unlock actuator 113. The pushback member, latch lever, emergency release rotor, full lock switch and pushback lock switch of assembly 117 are shown, but not numerically denoted for brevity. Being door status switches, the full and pushback lock switches can be deployed with their first contacts providing input to a DCU. Their second contacts can be wired into the DCLC trainline 13, but this is optional for the full lock switches as only their first contacts need be used to confirm to a DCU when the doors have been fully locked.~~

~~Referring again to Figures 4A-C illustrating first door lock assembly 44, latch lever 62 is pivotally connected at its upper end to the body of assembly 44 at a point above the right end of lock member 43. Latch lever 62 has a cam 66 (shown in dotted lines) on the other end of its pivot pin. Located at the lower end of this lever is the latch itself. Full lock switch 56 is positioned~~

behind pushback lock switch 58, with both being secured to the body of lock assembly 44. Pushback member 59 is pivotally connected to the body, just to the right of pushback lock switch 58. Unlock actuator 49 has its right end is secured to the body of assembly 44. The actuator has a push rod 51 extending from its left end. The leftmost end of push rod 51 connects by a pin to the upper left end of lock member 43 and within the channel joint of pushback member 59.

Designed to be pivoted about pin 45, lock member 43 features lock step 54, pushback step 55, cam receptor slot 68, and a lock arm formed as a part of its leftmost end. Cam receptor slot 68 is formed in the top side of lock member 43 near its right end, and pushback step 55 is formed on the bottom side of lock member 43 near its middle. Lock step 54 is formed in the lower right end of lock member 43.

Lock members 43 and 122 are disposed within first and second door lock assemblies 44 and 117, respectively, so as to be normally biased in the downward state. For first door lock assembly 44, this is best shown in Figure 4C. For second door lock assembly 117, it is best shown in Figure 5C. Specifically, starting with Figure 3B with reference to Figure 4A, as first door 42 is being moved rightward towards the CLOSE POSITION by motor 76 and drive mechanism 170, contact bracket 47 atop outer door hanger 46

~~eventually slides left to right underneath the bottom side of lock member 43. As outer door hanger 46 and door 42 therewith continue rightward, the protuberance 65 of contact bracket 47 encounters the left side of the lower end of latch 62 causing latch 62 to rotate counterclockwise. This counterclockwise rotation causes the cam 66 of latch 62 to rotate out of engagement with the cam receptor slot 68 of lock member 43. With its right end being disengaged from cam 66, lock member 43 then pivots clockwise about pin 45 so that its right end falls on top of bracket 47. As outer door hanger 46 and door 42 therewith close to within approximately 40 mm. of the CLOSE POSITION, the leftmost corner of bracket 47 is first caught by pushback step 55 due to the downward bias of lock member 43, as shown in Figure 4B. This causes pushback member 59 to pivot clockwise and engage the button of pushback lock switch 58. With its two contacts closed, switch 58 closes its portion of the DCLC trainline 38 and provides a pushback-locked signal to a DCU to indicate that the pushback lock 55 has engaged (i.e., member 43 has assumed the pushback-locked state). As motor 76 and drive mechanism 170 continue to close doors 42 and 110, the leftmost corner of contact bracket 47 moves through the pushback region between steps 55 and 54 and is eventually caught by lock step 54, as shown in Figure 4C. This causes lock member 43 to pivot clockwise further about pin 45 so that its leftwardly extending arm~~

~~engages the button of full lock switch 56. With its contact closed, switch 56 sends to a DCU a fully-locked signal indicating that the full lock 54 has now engaged. It is in this manner that lock member 43 assumes the fully-locked state wherein the leftmost corner of contact bracket 47 abuts against lock step 54 thereby preventing outer door hanger 46 and first door 42 therewith from being re-opened.~~

~~Due to the linkage of drive mechanism 170, second door 110 is moved leftward simultaneously with the rightward movement of first door 42. Specifically, starting again with Figure 3B with reference to Figure 5A, as second door 110 is being moved leftward towards the CLOSE POSITION, contact bracket 123 atop outer door hanger 121 eventually slides right to left underneath the bottom side of lock member 122. As outer door hanger 121 and second door 110 therewith continue leftward, the protuberance of bracket 123 encounters the right side of the lower end of the latch in assembly 117 causing that latch to rotate clockwise. This clockwise rotation causes the cam of that latch to rotate out of engagement with the cam receptor slot of lock member 122. With its left end being disengaged from the latch cam, lock member 122 then pivots counterclockwise about its pin so that its left end falls on top of bracket 123. As outer door hanger 121 and door 110 therewith close to within approximately 40 mm. of the CLOSE POSITION, the rightmost corner of~~

contact bracket 123 is first caught by the pushback step of lock member 122 due to the downward bias operating on it, as shown in Figure 5B. This causes the pushback member of assembly 117 to pivot counterclockwise and engage the button of its corresponding pushback lock switch. With its two contacts closed, this switch closes its portion of the DCLC trainline 38 and provides a pushback-locked signal to a DCU to indicate that the pushback lock of lock member 122 has engaged (i.e., member 122 has assumed the pushback-locked state). As motor 76 and drive mechanism 170 continue to close doors 110 and 42, the rightmost corner of contact bracket 123 moves through the pushback region between the steps of lock member 122 and is eventually caught by the lock step, as shown in Figure 5C. This causes the lock member 122 to pivot counterclockwise further about its pin so that its rightwardly extending arm engages the button of the full lock switch for assembly 117. With its contact closed, this switch sends to a DCU a fully-locked signal indicating that the full lock of lock member 122 has now engaged. It is in this manner that lock member 122 assumes the fully-locked state wherein its lock step serves as an abutment against the rightmost corner of contact bracket 123 thereby preventing the second door panel 110 from being re-opened. Moreover, due to the linkage of drive mechanism 170, whenever any

~~one of the lock members 43 and 122 is fully locked, both doors are prevented from opening.~~

~~U.S. Patent Application 09/099,260, now US Patent 6,032,416, discloses that biasing strips 52 and 120 on the inner edges 53 and 114 of doors 42 and 110, respectively, are important to the proper operation of first and second door lock assemblies 44 and 117. When moved to the point at which these two biasing strips actually contact each other, the doors 42 and 110 occupy the CLOSE POSITION shown in Figure 3. In order to fully lock the doors, however, a DCU must command motor 76 to rotate in the closing direction even further so that drive mechanism 170 closes the doors with sufficient force to compress the two biasing strips 52 and 120 together, albeit temporarily. Only with the biasing strips 52 and 120 in compression do the door panels close together far enough to reach the FULL LOCK POSITION in which lock members 43 and 122 drop into the aforementioned fully-locked states.~~

~~The button of full lock switch 56 is closed by the leftwardly extending arm of lock member 43 only when member 43 is placed in the fully-locked state shown in Figure 4C. The same applies to the full lock switch of second door lock assembly 117, as is shown in Figure 5C. When their buttons are closed, the full lock switches send to a DCU their respective fully-locked signals indicating that each of lock members have assumed the fully-locked state. Once~~

these fully-locked signals are received, a DCU can be used to deactivate motor 76.

Once motor 76 is deactivated, the doors 42 and 110 retreat to the HOME POSITION in which the outermost corners of contact brackets 47 and 123 forcibly abut against the full locks of lock members 43 and 122, respectively. This is because the biasing strips 52 and 120 decompress only partially when the motor is deactivated. As they are still under compression, the biasing strips 52 and 120 provide a load that is mechanically transmitted to the lock steps of both lock members 43 and 122. For example, with regard to first door lock assembly 44, this load is transmitted from the biasing strips through first door 42, through outer door hanger 46 to the leftmost corner of contact bracket 47 attached thereto. Consequently, the leftmost corner of contact bracket 47 is forcibly pressed against lock step 54 of lock member 43. Likewise, with regard to second door lock assembly 117, the rightmost corner of contact bracket 123 is forcibly pressed against the lock step of lock member 122. The load provided by the compression of the strips thus prevents the doors 42 and 110 from moving out of the HOME POSITION.

Notwithstanding use of emergency release rotor 64 as described below, the door hardware system 35 will permit the doors to be unlocked manually only under the following circumstances. Motor 76 must first be commanded to rotate in the closing direction so that

the doors close to the maximum possible extent, moving from the HOME POSITION beyond the FULL LOCK POSITION to the UNLOCK POSITION. Only by closing the doors to the UNLOCK POSITION are the biasing strips 52 and 120 compressed enough to relieve the mechanical load that otherwise keeps the outermost corners of contact brackets 47 and 123 engaged against the full locks of lock members 43 and 122, respectively. Each unlock actuator 49 and 113 must then be commanded to move its corresponding lock member upward to the unlocked state. Only with the mechanical load relieved are the unlock actuators 49 and 113 of door hardware system 35 able to move the lock members 43 and 122 to the unlocked state.

A DCU can be used to control the operation of the two unlock actuators 49 and 113. When energized to move lock member 43 upward to the unlocked state, unlock actuator 49 extends its push rod 51 from its left end. Due to its attachment to the upper left end of lock member 43, the push rod 51 forces lock member 43 to pivot counterclockwise about pin 45 so that its right end rises upward as shown in Figure 4A. As push rod 51 is moved leftward, the lock arm of lock member 43 disengages from the button of full lock switch 56. As it continues leftward, push rod 51 next pushes the channel joint of pushback member 59 further to the left thereby causing pushback member 59 to pivot counterclockwise and disengage from the button of pushback lock switch 58. With its contact open, full

~~lock switch 56 provides an indication to a DCU that lock member 43 is now in the unlocked state. Moreover, with its contacts opened, pushback lock switch 58 opens its portion of the DCLC trainline 38 and similarly provides an indication that member 43 is no longer in the pushback-locked state. Unlock actuator 113 of second door lock assembly 117 can be likewise energized to move lock member 122 upward to the unlocked state, as shown in Figure 5A.~~

~~Once it has been determined that lock members 43 and 122 are being held in the unlocked state and the doors can now be opened, motor 76 can be commanded to rotate in the opening direction. This would cause the first and second drive nuts of drive mechanism 170 to travel away from each other as the oppositely threaded screws 80 and 102 on which they respectively ride are rotated in the opening direction. Due to their interconnection with the drive nuts, via inner hangers 83 and 111, respectively, the door panels 42 and 110 open apart with their respective door hangers sliding along door hanger rod 88.~~

~~The operation of first door lock assembly 44 when the doors are being opened is best appreciated viewing Figure 3C with reference to Figures 4A and 4B. As first door 42 is being moved leftward, contact bracket 47 atop outer door hanger 46 slides right to left underneath the bottom side of lock member 43. As best appreciated from viewing Figures 4B and 4A in sequence, as the leftmost corner~~

~~of contact bracket 47 moves past pushback step 55, the protuberance 65 begins to interact with the latch of latch lever 62 causing the lever to rotate clockwise. As shown in Figure 4A, this clockwise rotation causes the cam 66 of lever 62 to rotate into engagement with the cam receptor slot 68 of lock member 47. With cam 66 of latch lever 62 now retained inside receptor slot 68, lock member 43 is now mechanically held in the unlocked state. Unlock actuator 49 can now be deenergized. Lock member 43 will remain in the unlocked state as long as the protuberance 65 of contact bracket 47 remains to the left of latch lever 62 (i.e., while first door 42 is open). Regarding the operation of second door lock assembly 117 when the doors are being opened, this is best appreciated viewing Figure 3C with reference to Figures 5A and 5B. The simultaneous opening of second door 110 and its effect on the relevant parts of assembly 117 are not described here for the sake of brevity. Suffice it to say that the latch lever and lock member 122 of second door lock assembly 117 are likewise effected by the protuberance of contact bracket 123 atop inner door hanger 111 attached to second door 110. Lock member 122 will remain mechanically held in the unlocked state by the cam of that latch lever as long as the protuberance of contact bracket 123 remains to the right of the latch lever of second door lock assembly 117 (i.e., while second door 110 is open).~~

U.S. Patent Application 09/099,260, now US Patent 6,032,416, also discloses a mechanical door pushback feature in door hardware system 35. With regard to first door 42, this pushback feature involves pushback position switch 60, contact strip 84, and lock member 43 of first door lock assembly 44. Connected across the third and fourth rod hangers 90 is a bracket, shown below center coupling 104 in Figure 3B. Attached to the underside of this bracket, just left of center, is pushback position switch 60. Connected to the lower section of inner door hanger 83 by means of a bracket is a rightwardly extending elongated contact strip 84, as best shown in Figure 3C. For first door 42, the pushback region may be defined as that limited range of movement for the door in which pushback position switch 60 is engaged by contact strip 84. Likewise, with regard to second door 110, this pushback feature involves pushback position switch 119, contact strip 118, and lock member 122 of second door lock assembly 117. Attached to the underside of the bracket spanning the third and fourth rod hangers 90, just right of center, is pushback position switch 119, as shown in Figure 3B. Connected to the lower section of inner door hanger 111 by means of a bracket is a leftwardly extending elongated contact strip 118, as shown in Figure 3C. For second door 110, the pushback region may be defined as that limited range of movement for the door in which switch 119 is engaged by contact strip 118.

~~Being door status switches, the pushback position switches 60 and 119 can be deployed so that their first contacts provide input to a DCU, with their second contacts wired into the DCLC trainline 38. Pushback position switch 60, when it is engaged by contact strip 84, closes its portion of the DCLC trainline 38 and provides to a DCU a door pushback signal indicating that first door 42 is in the pushback region. Likewise, pushback position switch 119, when it is engaged by strip 118, closes its portion of the DCLC trainline 38 and provides a door pushback signal indicating that second door 110 is in its pushback region. Moreover, the extent to which the doors can be parted when in the pushback region can be limited by lock members 43 and 122 to the PUSHBACK LOCK POSITION in which the outermost corners of contact brackets 47 and 123 respectively abut against the pushback locks of members 43 and 122, as shown in Figures 4B and 5B. Specifically, with lock members 43 and 122 in their pushback-locked states, each door can only be re-opened from its CLOSE POSITION as far as its PUSHBACK LOCK POSITION, a preset distance of typically 40 mm.~~

~~Figures 4B and 5B best illustrate the pushback-locked states of lock members 43 and 122, respectively, which limits the extent to which the doors may be opened when unlocked. This door pushback feature thus allows a passenger to slightly open the doors to~~

extract a garment, possession or even a body portion that has become caught between the closing doors.

More specifically, Figure 4B illustrates outer door hanger 46 of first door 42 in the PUSHBACK LOCK POSITION in which lock member 43 lies atop contact bracket 47 with its pushback step 55 abutting the leftmost corner of contact bracket 47. With lock member 43 placed in the pushback-locked state, its pushback step 55 thus limits the extent to which a passenger can open first door 42 leftward towards the OPEN POSITION. Moreover, as previously described, when its pushback lock 55 is engaged, lock member 43 causes pushback member 59 to close the contacts of pushback lock switch 58. Similarly, Figure 5B illustrates outer door hanger 121 of second door 110 in the PUSHBACK LOCK POSITION in which lock member 122 lies atop contact bracket 123 with its pushback step abutting the rightmost corner of contact bracket 123. With lock member 122 placed in the pushback-locked state, its pushback step limits the extent to which a passenger can open second door 110 rightward towards the OPEN POSITION. Moreover, when its pushback lock is engaged, lock member 122 causes the pushback member of assembly 117 to close the contacts of its corresponding pushback lock switch. In this manner, door operator 35 can keep a DCU apprised of whether the doors are in the pushback region by pushback position switches 60 and 119 and of whether lock members 43 and 122 are in their

~~pushback-locked states by their respective pushback lock switches. How these signals will be used ultimately depends on the particular DCU with which the door hardware system 35 is to be used.~~

~~The bi-parting doors of door hardware system 35 are thus mechanically self-locking doors. When moved from the OPEN POSITION, shown in Figure 2, into the pushback region, the doors are manually locked into the pushback region by the pushback steps of lock members 43 and 122, as shown in Figures 4B and 5B. The maximum extent to which the doors can be separated when in the pushback region is thus limited, typically to 80 mm. This feature effectively prevents a passenger from falling out of the railcar. The manner in which the door operator 35 may be controlled to implement this door pushback feature and others is dependent on the particular DCU with which the operator 35 is to be used. Finally, when moved further to the LOCK POSITION, the doors are fully self-locking in the HOME POSITION by the lock steps of lock members 43 and 122, as shown in Figures 4C and 5C.~~

~~The door hardware system 35 disclosed in U.S. Patent Application 09/099,260, now US Patent 6,032,416, also features a manually operated mechanism by which to unlock the doors in an emergency. For example, first door lock assembly 44 has an emergency release rotor 64, as best shown in Figures 4A-4C. It is rotatably connected to the body of first door lock assembly 44, just right of~~

latch 62. Emergency rotor 64 has lift cam 69 and push cam 70. Attached to the periphery of the rotor is one end of a flexible cord 72 whose other end is attached to the EXT EMER door release handle accessible to potential rescuers outside the railcar and, optionally, to the INT EMER door release handle accessible to passengers inside the railcar. The emergency release rotor, flexible cord and related parts of second door lock assembly 117, shown in Figures 5A-C, are not described for the sake of brevity. Suffice it to say that the emergency release rotors of the two door lock assemblies 44 and 117 can be manually activated through the same handle.

Regarding the operation of this manual emergency-open mechanism, emergency release rotor 64 rotates clockwise when cord 72 is pulled by manual activation of the handle(s). As best appreciated from Figure 4C, as rotor 64 is rotated, lift cam 69 soon comes into contact with the rightmost tip of lock member 43. The purpose of lift cam 69 is to lift lock member 43 to the unlocked state, i.e., upward and away from contact bracket 47 fixed atop outer door hanger 46. Further rotation of the rotor causes push cam 70 to push contact block 48 of bracket 47 to the left a predetermined distance, typically 9 mm. In pushing contact block 40, push cam 70 also opens first door 42 to the same extent, as the door is interconnected to contact bracket 47 via outer door hanger 46. As

~~shown in Figures 5A-C, second door 110 opens in the same manner and to the same extent via the emergency release rotor and related parts of second door lock assembly 117. With the bi-parting doors 42 and 110 both slightly opened, the passengers can not only see that the doors are unlocked but also obtain leverage to manually open the doors further apart to allow egress from the railcar 41.~~

Illustrated in Figures ~~6~~4 through 1~~4~~2 are the essential details of an intelligent door controller unit (IDCU) and related inventions. The IDCU is preferably organized into three modules: a CPU card 200, a motor driver & input/output (MD-I/O) card 300, and a power supply card 400, as best shown in Figures ~~6~~4 and ~~7A-B~~5A-B. Each of these cards features a printed circuit board onto which an industry-standard bus structure, such as the PC-104 embedded processor interface, has been laid out. A simplified representation of the bus structure is shown in Figures ~~7A-B~~5A-B, with a more detailed depiction shown in Figures ~~10A-C~~8A-C. It is into this bus structure that the addressable components of the invention have been incorporated.

Designed to serve as the motherboard for the IDCU, the MD-I/O card 300 has upwardly disposed connectors built into its bus structure. Being physically linked to the motherboard via such connectors, the CPU and power supply cards 200 and 400 can thus be

stacked horizontally atop the MD-I/O card 300. This allows the IDCU to be contained compactly within a single enclosure. As explained in greater detail below, this modular architecture also allows more capability to be added to the IDCU merely by connecting additional cards to the vertical bus structure by which the desired functions can be implemented.

The CPU card 200 includes a standard serial port 210, databus memory buffer circuitry 220, and a microprocessor 230 accompanied by the appropriate volatile and non-volatile memories to store data and programming code and by various complex programmable logic devices (CPLDs) to perform CPU-type functions such as address decoding and buffering.

As best shown in Figures ~~7A-B~~5A-B and ~~10A-C~~8A-C, among other components, the MD-I/O card 300 includes a novel optoisolator device 310, several CPLDs, a motion control (digital signal) processor 320 (DSP chip), an H-bridge amplifier 330, a seven segment display 340, and a tone/audio amplifier 350. Three CPLDs are critical to the operation of the MD-I/O card 300: the ADD-CPLD, the I/O-CPLD and the MC-CPLD. The ADD-CPLD handles the address decoding functions. The I/O-CPLD handles the input and output functions of the IDCU. The MC-CPLD, in conjunction with the DSP chip, handles the motion control functions inclusive of controlling the H-bridge amplifier 330 to drive the motor 76 of the door

operator. These CPLDs are preferably in-system-programmable (ISP) devices. Well known in the electronic arts, each CPLD is capable of being programmed/reprogrammed within the bus structure of the circuit into which it has been incorporated. Each CPLD also features in-system diagnostic capabilities, meaning that each is capable of storing data about its own operations and reporting such data to the CPU card when queried for same as part of the diagnostic tests.

The ADD-CPLD is incorporated into the bus structure as shown in Figure ~~10B~~8B. It can take the form of an ISP version of the industry standard GAL 22v10, such as the one manufactured by the Lattice Semiconductor Corporation. The address decoder chip monitors the addresses that are issued by the CPU. Should the CPU fail in such a way that it issues addresses outside a predetermined range, the ADD-CPLD will cause the MC-CPLD to shutdown in a safe manner and, optionally, cause the warning lamp outside the affected doorway to flash. Likewise, the CPU monitors the address and data buses for erroneous conditions or faulty data issued by any of the CPLDs or the motion control processor. Should the CPU detect such errors, it can likewise cause a safe shutdown of the IDCU.

An important feature of the address decoder chip is that it can be reprogrammed at any time to support different address groups. This feature allows multiple MD-I/O cards to be connected

off of one CPU card 200. An example of the logic programmed into the ADD-CPLD is illustrated in Figure 1~~3~~1.

As an address decoder, the function of the ADD-CPLD is relatively simple in that it has only to produce six address strobe pulses for the address bus on the MD-I/O card. Each of the address strobes is configured to cover two address locations, each giving a total addressing range of twelve bytes. The starting address location was tentatively set at 300 (hex), as it is relatively unused by other PC devices. Considering that the design is based on an ISP chip, the addressing can be changed at any time as conditions dictate. To be compliant with the IBM PC I/O specification, only sixteen of the twenty four I/O address lines are decoded, the remaining eight lines will produce 256 echo locations throughout the memory map of the IDCU. ~~The memory map and register list for the addressable components of the IDCU is shown in Figures 15A-C.~~

The I/O CPLD is the component through which the central command signals and the local door hardware signals are input into the IDCU. As can be seen from Figures ~~6~~4, ~~7A-B~~5A-B, and ~~10A-C~~8A-C, the I/O-CPLD chip serves as the interface between the main control components of the IDCU and the CDC of the transit authority. The I/O-CPLD can take the form of the ISP-2064 chip manufactured by the Lattice Semiconductor Corporation.

The I/O CPLD is preferably deployed with the novel optoisolator device 310, also referred herein as the mirror-image optoisolator circuitry. It is well known, of course, that all of the central command inputs are considered extremely safety critical because a fault anywhere in the input path that these signals follow into a DCU can cause given rise to serious problems within any door system. The I/O-CPLD and the optoisolator device 310 together serve to monitor and verify the central command signals that the IDCU receives from the CDC.

As noted earlier, the IDCU can accept central command signals from either the discrete trainlines (i.e., a hard-wired switch interface) or an optional serial communications link. For example, regarding the discrete trainlines, the central command inputs can be conveyed to the IDCU via a single-switched or a doubled-switched input format. In the single-switched format, one line is activated and its associated return line (commonly the ground) is hardwired to the CDC. In the doubled-switched format, both the input line and its associated return are activated together at the CDC. When not in use, both lines are shorted together to reduce the chance of unwanted bias voltages or ground loops from triggering a door control signal.

The optoisolator device 310 optically isolates the IDCU from the discrete trainlines whether conveyed via the single-switched or

the doubled-switched input format. It is well known that the discrete trainlines are susceptible to picking up rather high voltage spikes from the environment in which they are used. Transit authorities thus require optical isolation because it protects the IDCU from such high voltage spikes; spikes that could otherwise cause the doors to operate improperly and even damage the electronics. Once the central command inputs are received by the optoisolator device 310, they are clamped and filtered, as best shown in Figure ~~11~~9, to reduce the possibility of transients from getting into the IDCU via the I/O-CPLD. For each input line, an input-voltage decoupler is used to minimize the effects of low-voltage DC bias signals. In addition, the values of the input circuits are tailored to suit the voltage requirements of the train. Furthermore, the line filters are tuned to minimize the electrical noise spectrum expected to be seen by the IDCU.

In addition to monitoring and verifying the authenticity of all trainline inputs, the CPU and I/O-CPLD together route the incoming central command inputs and local door hardware inputs to the appropriate component in the IDCU so that the required task(s) can be performed. The I/O-CPLD is also programmed to handle various output functions for the IDCU. The following is merely a brief list of the functions that the I/O-CPLD can be programmed to perform: filter the central command signals received from the

trainlines; monitor and decode all central command inputs; detect erroneous signals; generate CPU I/O interrupt signals; monitor various passenger activated switches; control speaker/beepers on MD-I/O card; control the warning lamp(s) outside the doorway(s); monitor power-supply voltages; monitor the I/O output fault status; test the optocouplers; test the input and encoder connectors for proper connection; transfer status and interrupt data to the MC-CPLD; generate the clock pre-scalar signals; and control one of the two unlock actuators 49 or 113 of the two door lock assemblies 44 and 117. An example of the logic programmed into the I/O-CPLD is illustrated in Figures 1~~2~~0A-C.

Referring now to Figures ~~6~~4, ~~7A-B~~5A-B and ~~10A-C~~8A-C, the MC-CPLD, in conjunction with the motion control processor (DSP chip), handles the motion control functions inclusive of controlling the H-bridge amplifier 330 to drive the motor 76 of the door operator. The MC-CPLD and the DSP chip 320 can take the form of the ISP-1032 and LM629 chips manufactured by the Lattice Semiconductor Corporation and National Semiconductor Corporation, respectively. Like the aforementioned CPLDs, these chips are commercially available devices. The following specification sheets for these devices are incorporated herein by reference: ADD-CPLD (ISP22lv_03 sheet dated March 1998), I/O-CPLD (2064_04 sheet dated October 1998) and MC-CPLD (1032_05 sheet dated October 1998)

published by Lattice Semiconductor Corporation; and the LM629 chip (TL/H/9219 dated February 1995) published by the National Semiconductor Corporation.

The MC-CPLD and various related circuits and components are disposed on the MD-I/O card 300 as shown in Figures 1~~4~~2A-E. The output control circuits in the MC-CPLD, as well as those in the I/O-CPLD, have built-in short circuit protection, which will shutdown the output operations should a fault be detected. Implemented primarily within the MC-CPLD chip are the data/address control logic as shown in Figure 1~~4~~2A, the current feedback and deadtime circuitry shown in Figure 1~~4~~2B, the encoder monitoring circuitry shown in Figure 1~~4~~2C, and the interrupt control logic shown in Figure 1~~4~~0E. The access key circuitry, the watchdog timer circuitry and the motor control circuitry for the H-bridge, shown in Figures ~~6~~4, ~~7B~~5B and 1~~4~~2D, are implemented both internal and external to the MC-CPLD. The integration capacitor circuitry is external to the MC-CPLD, as is best shown in Figure ~~7B~~5B. This circuitry is used to monitor the power/wattage in the motor 76 during overload conditions, otherwise it is discharged.

Regarding the motion control processor 320, the LM629 chip was selected for the control of the motor. This chip was designed to operate in a stand-alone mode of operation where there are no supporting RAM or ROM chips for the DSP low level program. This

makes the DSP chip nearly impervious to internal crashes and although it is a complex 32 bit device, it has an inherent ruggedness that is not surpassed with any other device. It is well suited to electrically noisy environments where safety is the utmost consideration. This chip also is capable of serving as a component common to a variety of different door control system architectures. This is possible due to the tremendous amount of control range built into the DSP chip 320.

The LM629 is preferred because it lends itself to a motor control design that is almost entirely digital in operation. Because no analog control loops are used (e.g., linear current & tachometer feedback), the IDCU is relatively immune to noise causing position/velocity errors in the operation of the doors.

Figures ~~6~~4, ~~7B~~5B and ~~10C~~8C best illustrate the H-bridge amplifier 330. Driven by the motor current circuitry in the MC-CPLD via pwm and direction signals, the H-bridge amplifier 330 includes optical isolation circuitry, level shifting circuitry, and field effect transistors (FETs) with which to drive the motor. The lower two FETs are current sensing devices. They provide to the motor current and power monitoring circuitry in the MC-CPLD feedback as to the magnitude of the current in the motor 76. This analog feedback is used only to protect the H-bridge circuitry 330 and the motor 76 during dynamic braking. The IDCU does not use

current feedback to detect obstructions. Circuitry is also employed to protect the components of the H-bridge circuitry 330 and the motor 76 from surge voltages and other adverse electrical influences.

During the open stroke, the IDCU also performs an obstruction detection operation. The level of sensitivity can be set differently from that of the close cycle depending upon the importance for shorter cycle times. During the open stroke, the lock members 43 and 122 are mechanically latched up thereby allowing the power to be removed from their respective solenoids. This method extends the life expectancy of the solenoids and also reduce the power consumed by the IDCU.

The IDCU also makes use of four limit switches to help qualify the real position of the doors. These switches are best shown in Figures ~~6~~4 and ~~7A-B~~5A-B. These switches include (1) two door close limit switches (one per door panel) showing the doors are in the closed position; (2) two pushback lock switches 58 each indicating that its lock member is partially engaged, i.e., in the pushback-locked state; (3) two full lock switches 56 each indicating that its lock member is fully engaged, i.e., in the fully-locked state. In this state, the full lock switches indicating to the IDCU that the power need no longer be supplied to the motor 76.

While the presently preferred embodiment for carrying out the instant invention has been set forth in detail, those persons skilled in the digital circuit art to which this invention pertains will recognize various alternative ways of practicing the invention without departing from the spirit and scope of the patent claims appended hereto.

ABSTRACT

A programmable system and a self-locking memory circuit for a ~~tri state~~tristate data bus having multiple bit lines. The circuit includes a non-inverting amplifier chip for connection to one of the bit lines and a resistor having a predetermined electrical resistance connected across the amplifier chip. The chip and resistor provide a predetermined impedance to the flow of electrical current in the self-locking circuit. The circuit changes its state when the current of the latest information on a bit line builds or lowers above or below threshold levels of the self-locking circuit. The ~~tri state~~tristate data bus may be connected between a digital signal processor (DSP), a complex programmable logic device (CPLD) and a central processing unit (CPU) operating at different rates or speeds.